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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,819	11/25/2003	Emil Lambrache	ATM-267	9370

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EXAMINER	
MARTINEZ, DAVID E	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 09/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/722,819	LAMBRACHE ET AL.	
	Examiner	Art Unit	
	David E. Martinez	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/7/05, 3/12/04.* 3/9/04 DM
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (hereinafter AAPA).

1. With regards to claim 1, AAPA teaches a serial peripheral interface apparatus [fig 1], comprising:

a plurality of serial data-transfer means coupled together for transferring data serially [fig 1 elements 102, 110 – page 2 lines 16-20];

buffer means coupled to said plurality serial data-transfer means for storing a subsequent data byte to be transferred [page 1 lines 13-25];

counter means coupled to said buffer means and said plurality of serial data-transfer means for checking a status of a data transmission within said apparatus [page 3 lines 9-11]; and

control means coupled to said buffer means, said counter means, and said plurality of data transferring means for controlling said data transmission within said apparatus and for enabling a loading of said subsequent data byte into said buffer means [page 1 lines 13-25, page 2 lines 8-10, lines 21-22 and page 3 lines 11-14]

AAPA teaches all of the above limitations, but is silent as to the control means reviewing a status of said counter means and a status of said buffer means. However, AAPA teaches that control means can 'pinpoint the exact moment when to request a new data byte', it waits for a

current data byte transmission to complete in order to avoid write collisions, and signals a CPU when it is ready to receive a subsequent byte. It can be concluded that the operation by the control means to check the status of both the counter means and the buffer means take place, since it is shown that the control means know when a transfer has been completed. If there are any bits accounted/unaccounted for during a data transmission, and seeing how full or empty the buffer is, are conventional conditions used to determine if a transmission is taking place or if it has been completed. The control means know when to transfer a subsequent byte, which happens after it knows that a previous transfer operation is complete as disclosed by AAPA for the benefit of avoiding a write collision [page 1 lines 13-25, page 2 lines 8-10, lines 21-22 and page 3 lines 11-14].

It would have been obvious to one of ordinary skill in the art at the time of the invention to see that the control means actually review a status of said counter means and a status of said buffer means for the benefit of avoiding a write collision as explained above.

2. With regards to claim 2, AAPA teaches the serial peripheral interface apparatus of claim 1, wherein a plurality of serial data-transfer means further comprises a first serial data-transfer means serving as a serial master [fig 1 element 102] with an output coupled to a second serial data-transfer means serving as a serial slave [fig 1 element 110 – page 2 lines 16-20].

3. With regards to claim 3, AAPA teaches the serial peripheral interface apparatus of claim 2, wherein said first serial data-transfer means [fig 1 element 102] further comprises a multiplexer means [fig 1 element labeled 'MUX' inside element 102] coupled to a latching means [fig 1 element labeled 'F.F.' inside element 102].

4. With regards to claim 4, AAPA teaches the serial peripheral interface apparatus of claim 2, wherein said second serial data-transfer means [fig 1 element 110] further comprises a

multiplexer means [fig 1 element labeled 'MUX' inside element 110] coupled to a latching means [fig 1 element labeled 'F.F.' inside element 110].

5. With regards to claim 5, AAPA teaches the serial peripheral interface of claim 1 further comprising a parallel data-transfer means serving as a parallel slave, the parallel data-transfer means coupled to an output of one of said serial data-transfer means.[fig 1 element 130, output line from element 102 is an input to element 130, page 2 lines 16-20].

6. With regards to claim 6, AAPA teaches the serial peripheral interface apparatus claim 5, wherein said parallel slave data-transfer means further comprises a latching means [fig 1 element labeled 'F.F.' inside element 130].

7. With regards to claim 7, AAPA teaches the serial peripheral interface apparatus of claim 1, wherein said control means further controls a loading of said subsequent data byte to said plurality of serial data-transfer means [page 1 lines 13-25, page 2 lines 8-10, lines 21-22 and page 3 lines 11-14].

8. With regards to claim 8, AAPA teaches the serial peripheral interface apparatus of claim 1, wherein the control means is responsive to the status of the counter means for permitting loading of data bytes into said buffer means only until a time slot in which a fourth bit of a present data byte is transferred [page 1 lines 13-25, page 2 lines 8-10, lines 21-22 and page 3 lines 11-14].

9. With regards to claims 9 and 16, a serial peripheral interface apparatus [fig 1], comprising:

a plurality of shift registers coupled together for transferring data serially [fig 1 elements 102, 110 – page 2 lines 16-20];

a write buffer coupled to said plurality of shift registers [page 1 lines 13-25];

bit counter coupled to said plurality of shift registers for keeping track of a bit field of a data byte being transferred through said apparatus [page 3 lines 9-11]; and

a finite state machine controller coupled to said apparatus for controlling data transmission therethrough and for enabling a loading of a subsequent data byte into said write buffer by checking a status of said counter and a status of said write buffer [page 1 lines 13-25, page 2 lines 8-10, lines 21-22 and page 3 lines 11-14 under the same reasons as those set forth in claim 1 above].

10. With regards to claim 10, AAPA teaches the apparatus of claim 9, wherein said plurality of shift registers further comprises a serial master shift register [fig 1 element 102], a serial slave shift register [fig 1 element 110 – page 2 lines 16-20] coupled to an output of said serial master shift register for transferring data serially, and a parallel slave shift register coupled to said output of said serial master shift register [fig 1 element 130, output line from element 102 is an input to element 130, page 2 lines 16-20].

11. With regards to claim 11, AAPA teaches the serial peripheral interface apparatus of claim 10, wherein said master serial shift register [fig 1 element 102] further comprises a multiplexer [fig 1 element labeled 'MUX' inside element 102] coupled to a clocked flip-flop [fig 1 element labeled 'F.F.' inside element 102].

12. With regards to claim 12, AAPA teaches the serial peripheral interface apparatus claim 10, wherein said serial slave shift register [fig 1 element 110] further comprises a multiplexer [fig 1 element labeled 'MUX' inside element 110] coupled to a clocked flip-flop [fig 1 element labeled 'F.F.' inside element 110].

13. With regards to claim 13, AAPA teaches The serial peripheral interface apparatus of claim 10 wherein said parallel slave shift register further comprises a clocked flip-flop [fig 1 element labeled 'F.F.' inside element 130].

14. With regards to claim 14, AAPA teaches the serial peripheral interface apparatus of claim 10, wherein said finite state machine controller further controls a loading of said data byte to said plurality of shift registers [page 1 lines 13-25, page 2 lines 8-10, lines 21-22 and page 3 lines 11-14].

15. With regards to claim 15, AAPA teaches The serial peripheral interface apparatus of claim 10 wherein the finite state machine controller is responsive to a status of the bit counter so as to permit loading of a subsequent data byte into the write buffer only until a time slot in which a fourth bit of a present data byte is transferred [page 1 lines 13-25, page 2 lines 8-10, lines 21-22 and page 3 lines 11-14].

16. With further regards to claim 16, AAPA teaches a microcontroller comprising:

a central processing unit [page 3 lines 1-14];

a bus interface coupled to said central processing unit [page 3 lines 1-14];

a memory module coupled to and in communication with said central processing unit via said bus interface [page 3 lines 1-14];

- Examiner notes that the AAPA (Figure 1) differs from the Applicant's invention (Figure 2), by the 2nd parallel write buffer, element 250. The parallel write buffer – element 250 - has not been incorporated into independent claims 1, 9, and 16, and thus why AAPA reads on them.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Martinez whose telephone number is (571) 272-4152. The examiner can normally be reached on 8:30-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popovici can be reached on (571) 272-4083. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DEM